WHAT IS CLAIMED IS:

1. A nonvolatile memory comprising:

a single crystal semiconductor;

a source region, a drain region, and an active region being formed in the single crystal semiconductor;

a plurality of impurity regions provided locally in the active region; and

at least a substantially intrinsic channel forming region interposed between the impurity regions.

2. A nonvolatile memory comprising:

a substrate having an insulating surface;

a semiconductor thin film provided over the substrate, said semiconductor film being substantially regarded as a single crystal;

a source region, a drain region, and an active region in the semiconductor thin film;

a plurality of impurity regions provided locally in the active region; and

at least a substantially intrinsic channel forming region interposed between the impurity regions.

3. A nonvolatile memory comprising:

a single crystal semiconductor;

a source region, a drain region, and an active region being formed in the single crystal semiconductor;

a plurality of impurity regions provided locally in the active region; and

at least a substantially intrinsic channel forming region interposed between the impurity regions,

wherein each of said impurity regions comprises an element selected from group 13 or group 15.

4. A nonvolatile memory comprising:

a single crystal semiconductor;

a source region, a drain region, and an active region being formed in the single crystal semiconductor;

a plurality of impurity regions provided locally in the active region; and

at least a substantially intrinsic channel forming region interposed between the impurity regions,

wherein each of said impurity regions comprises an element selected from group 13 or group 15,

wherein said impurity regions prevent a depletion layer from expanding from the drain region toward the source region.

5.A nonvolatile memory comprising:

a substrate having an insulating surface;

a semiconductor thin film provided over the substrate, said semiconductor film being substantially regarded as a single crystal;

a source region, a drain region, and an active region in the semiconductor thin film;

a plurality of impurity regions provided locally in the active region; and

at least a substantially intrinsic channel forming region interposed between the

impurity regions,

wherein each of said impurity regions comprises an element selected from group 13 or group 15.

6. A nonvolatile memory comprising:

a substrate having an insulating surface;

a semiconductor thin film provided over the substrate, said semiconductor film being substantially regarded as a single crystal;

a source region, a drain region, and an active region in the semiconductor thin film;

a plurality of impurity regions provided locally in the active region; and

at least a substantially intrinsic channel forming region interposed between the impurity regions,

wherein each of said impurity regions comprises an element selected from group 13 or group 15,

wherein said impurity regions prevent a depletion layer from expanding from the drain region toward the source region.

7. A memory according to claim 1, wherein each of the impurity regions formed from the source region to the drain region has a stripe shape.

8. A memory according to claim 1, wherein an element is comprised in each of the impurity regions at a concentration in the range of 1×10^{17} to 5×10^{20} atoms/cm^3.

9. A memory according to claim 2, wherein the substrate is a crystallized glass

substrate with an insulating film on a surface thereof.

10. An electronic apparatus including nonvolatile memory as a recording medium, said nonvolatile memory comprising:

a single crystal semiconductor;

a source region, a drain region, and an active region being formed in the single crystal semiconductor;

a plurality of impurity regions provided locally in the active region; and

at least a substantially intrinsic channel forming region interposed between the impurity regions.

11. A memory according to claim 2, wherein each of the impurity regions formed from the source region to the drain region has a stripe shape.

12. A memory according to claim 3, wherein each of the impurity regions formed from the source region to the drain region has a stripe shape.

13. A memory according to claim 4, wherein each of the impurity regions formed from the source region to the drain region has a stripe shape.

14. A memory according to claim 5, wherein each of the impurity regions formed from the source region to the drain region has a stripe shape.

15. A memory according to claim 6, wherein each of the impurity regions formed from the source region to the drain region has a stripe shape.

16. A memory according to claim 2, wherein an element is comprised in each of the impurity regions at a concentration in the range of 1×10^{17} to 5×10^{20} atoms/cm^3.

17. A memory according to claim 3, wherein the element is comprised in each of the impurity regions at a concentration in the range of 1×10^{17} to 5×10^{20} atoms/cm^3.

18. A memory according to claim 4, wherein the element is comprised in each of the impurity regions at a concentration in the range of 1×10^{17} to 5×10^{20} atoms/cm^3.

19. A memory according to claim 5, wherein the element is comprised in each of the impurity regions at a concentration in the range of 1×10^{17} to 5×10^{20} atoms/cm^3.

20. A memory according to claim 6, wherein the element is comprised in each of the impurity regions at a concentration in the range of 1×10^{17} to 5×10^{20} atoms/cm^3.

21. A memory according to claim 5, wherein the substrate is a crystallized glass substrate with an insulating film on a surface thereof.

22. A memory according to claim 6, wherein the substrate is a crystallized glass substrate with an insulating film on a surface thereof.

23. An electronic apparatus including nonvolatile memory as a recording medium, said nonvolatile memory comprising:

a substrate having an insulating surface;

a semiconductor thin film provided over the substrate, said semiconductor film

being substantially regarded as a single crystal;

a source region, a drain region, and an active region in the semiconductor thin film;

a plurality of impurity regions provided locally in the active region; and

at least a substantially intrinsic channel forming region interposed between the impurity regions.